



Invited Talk, Center for Energy-Efficient Computing and Applications

ROBUST SYSTEM DESIGN: FROM CLOUDS TO NANOTUBES

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ABSTRACT: Today's mainstream electronic systems typically assume that transistors and interconnects operate correctly over their useful lifetime. With enormous complexity and significantly increased vulnerability to failures compared to the past, future system designs cannot rely on such assumptions. At the same time, there is explosive growth in our dependency on such systems.

Robust system design is essential to ensure that future systems perform correctly despite rising complexity and increasing disturbances. For coming generations of silicon technologies, several causes of hardware failures, largely benign in the past, are becoming significant at the system-level. Furthermore, emerging nanotechnologies such as carbon nanotubes are inherently highly subject to imperfections.

This talk will address the following major robust system design goals:

- New approaches to thorough test and validation that scale with tremendous growth in complexity.
- Cost-effective tolerance and prediction of failures in hardware during system operation.

• A practical way to overcome substantial inherent imperfections in emerging nanotechnologies.

Significant recent progress in robust system design impacts almost every aspect of future systems, from ultralarge-scale networked systems, all the way to their nanoscale components.

BIOGRAPHY: Professor Subhasish Mitra directs the Robust Systems Group in the Department of Electrical Engineering and the Department of Computer Science of Stanford University, where he is the Chambers Faculty Scholar of Engineering. Before joining Stanford, he was a Principal Engineer at Intel Corporation. He received Ph.D. in Electrical Engineering from Stanford University.

Prof. Mitra's research interests include robust system design, VLSI design, CAD, validation and test, and emerging nanotechnologies. Prof. Mitra's honors include the Presidential Early Career Award for Scientists and Engineers from the White House, the highest U.S. honor for early-career outstanding scientists and engineers, Terman Fellowship, IEEE CAS/CEDA Pederson Award for the IEEE Transactions on CAD Best Paper, and the Intel Achievement Award, Intel's highest corporate honor. He and his students presented award-winning papers at several major conferences: IEEE/ACM Design Automation Conference, IEEE International Test Conference, IEEE VLSI Test Symposium, Intel Design and Test Technology Conference, and the Symposium on VLSI Technology. At Stanford, he was honored several times by graduating seniors "for being important to them during their time at Stanford."

Prof. Mitra has served on numerous conference committees and journal editorial boards. Recently, he served on the Defense Advanced Research Projects Agency's (DARPA) Information Science and Technology (ISAT) Board as an invited member. He is a Fellow of the IEEE.