

Invited Talk, Center for Energy-Efficient Computing and Applications

MODERN STATE RETENTION TECHNIQUES FOR POWER GATING DESIGN

Prof. Mark Po-Hung Lin National Chung Cheng University, Taiwan 2015年9月18日 星期五 10:30am 理科五号楼410会议室



ABSTRACT: As the semiconductor technology advances to nanometer era, leakage power becomes more and more critical in nanoscale integrated circuits. Power gating has been commonly adopted by shutting down the idle blocks for standby leakage power reduction. In order to keep flip-flop states during the sleep mode, applying retention registers is one of the most effective and efficient approaches. Instead of replacing each flip-flop in a power-gated circuit with a single-bit retention register (SBRR), recent research has shown that applying multi-bit retention registers (MBRRs) can effectively reduce the storage size, and hence save more chip area and leakage power. This talk will first give a brief overview among different flip-flop state retention techniques. Based on MBRRs, the design optimization problem as well as the corresponding solutions will be further introduced.

BIOGRAPHY: Mark Po-Hung Lin received the B.S. and M.S. degrees in electronics engineering from National Chiao Tung University (NCTU), Hsinchu, Taiwan, respectively, and the Ph.D. degree in the Graduate Institute of Electronics Engineering, National Taiwan University (NTU), Taipei, Taiwan. He has been with the Department of Electrical Engineering, National Chung Cheng University, Chiayi, Taiwan, since 2009, where he is currently an Associate Professor. He was with SpringSoft, Inc. (acquired by Synopsys in 2012) during 2000–2007 as an Engineer, a Senior Engineer, an Associate Manager, and a Technical Manager. He was a Visiting Scholar with the University of Illinois at Urbana-Champaign, Champaign, IL, USA, during 2007–2009, and a Humboldt Research Fellow with the Technical University of Munich (TUM), Germany, during 2013–2015. His current research interests include low-power circuit and system design optimization, and design automation for analog/mixed-signal integrated circuits. Dr. Lin was the recipient of Humboldt Research Fellowship for Experienced Researchers, IEEE Tainan Section Macronix Award, IEEE Tainan Section Best GOLD Member Award, Distinguished Young Scholar Award of Taiwan IC Design Society, Outstanding Young Electrical Engineer Award of the Chinese Institute of Electrical Engineering, and Distinguished Young Faculty Award of National Chung Cheng University.