As the semiconductor industry enters the era of extreme scaling (1x-nm), IC design and manufacturing challenges are exacerbated, which calls for increasing design and technology co-optimization for performance, power, manufacturability, and so on. Design for X (DFx, where X can mean power, performance, manufacturability/yield, reliability, security, ...) requires cross-layer information feed-forward and feed-back, to enable the overall design and manufacturing closure and optimization. This talk will first present some key challenges and practices how to enable DFx from mask synthesis to standard cell and physical design, dealing with multiple patterning lithography, and leveraging machine learning, etc. As new process technologies being proposed (e.g., new materials) and new design requirements (e.g., reliability and security) popping up, we expect to see many new challenges and opportunities for synergistic DFx. The talk will also cover some DFx needs for emerging technologies such as nanophotonic integration and emerging applications such as FPGA.

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