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Perspectives of Racetrack Memory Based on Current-Induced Domain Wall Motion: From Device to System

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***Abstract*—Current-induced domain wall motion (CIDWM) is regarded as a promising way towards achieving emerging high-density, high-speed and low-power non-volatile devices. Racetrack memory is an attractive concept based on this phenomenon, which can store and transfer a series of data along a magnetic nanowire. Although the first prototype has been successfully fabricated, its advancement is relatively arduous caused by certain technique and material limitations. Particularly, the storage capacity issue is one of the most serious bottlenecks hindering its application for practical systems. In this paper, we present two alternative solutions to improve the capacity of racetrack memory: magnetic field assistance and chiral domain wall (DW) motion. The former one can lower the current density for DW shifting; the latter one can utilize materials with low resistivity. Both of them are able to increase the nanowire length and allow higher feasibility of large-capacity racetrack memory. Furthermore, system level simulation shows that a racetrack memory based cache can improve system performance by about 15.8% and significantly reduces the energy consumption, compared to the SRAM counterpart.**

Keywords – Racetrack memory; Magnetic field assistance; Chiral domain wall motion; L2 cache.

I. INTRODUCTION

Recent progress of technique and material makes magnetic domain wall (DW) motions be regarded as a promising way to achieve non-volatile logic and memory devices [1]. In particular, due to the prospects of facility, high speed and low power, current-induced domain wall motion (CIDWM) draws further attentions from academics and industries. Racetrack memory is one of the most attractive applications based on this phenomenon [2-3]. In the basic structure, a series of magnetic domains move along magnetic nanowires, driven by a spin polarized current. Thanks to the well-defined nanowires, racetrack memory demonstrates an obvious potential in term of scalability. However, the path of its realization is arduous. For example, the prototype firstly fabricated was based on the materials with in-plane magnetic anisotropy, which cannot provide a sufficient thermal stability for further miniaturization [4]. Furthermore, the high values of DW shifting critical current and material resistivity limit the capacity of racetrack memory [5-6]. These challenges incent the motivations of both physical and material scientists.

Firstly, in order to overcome the issue of thermal stability, materials with perpendicular magnetic anisotropy (PMA) have being intensively studied and can offer various other performance improvements compared with those with in-plane magnetic anisotropy, such as lower DW nucleation critical current and higher DW shifting speed [7-8]. Secondly, it was demonstrated that, due to Walker breakdown effect, magnetic field could trigger the CIDWMs below intrinsic current threshold [9]. Magnetic field can thus be one of alternative solutions to handle the problem of high DW shifting current. Thirdly, chiral DW motions have been discovered to allow a high efficiency in terms of magnetization switching and DW shifting, compared with conventional spin transfer torque (STT) based CIDWMs [10-14]. This phenomenon is derived from spin-orbit torque (SOT). Thanks to low resistivity of material inducing SOI, chiral DW motions can overcome the aforementioned high resistivity drawback.

In this paper, we present two racetrack memory device structures based on new mechanisms: magnetic field assistance and chiral DW motions. These two implementations can improve the capacity of racetrack memory. By using SPICE compatible electrical model [15-17], mixed simulations and performance analyses are performed. Beyond the device and circuit design, the system level investigations are also performed. It demonstrates that a racetrack memory based cache can outperform traditional SRAM based cache, in respect of performance and energy consumption.

In section II, we introduce briefly the basic structure and theory of racetrack memory. Two capacity-improving solutions, magnetic field assistance and chiral DW motions, will be presented in section III. The system-level study is then detailed. At last, concluding remarks and perspectives are discussed in section V.

II. RACETRACK MEMORY INTRODUCTION

As shown in Fig. 1, a basic cell of racetrack memory is composed of three parts, i.e. write head, read head and storage nanowire. The write and read heads can be constructed by magnetic tunnel junctions (MTJs), which facilitate integration with CMOS writing and reading circuits. Data, in the form of magnetic domains, are stored along the magnetic nanowire. Different magnetic domains are separated by DWs, which can

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be pinned by artificial potentials or constrictions when no current is applied. As the distance between adjacent DWs can be extremely short, this concept can achieve a considerably high storage density. With respect to structural parts, three circuits are used to generate currents accordingly. Iw and Ir execute DW nucleation and detection respectively. Ish drives the DWs or data from write head to read head.

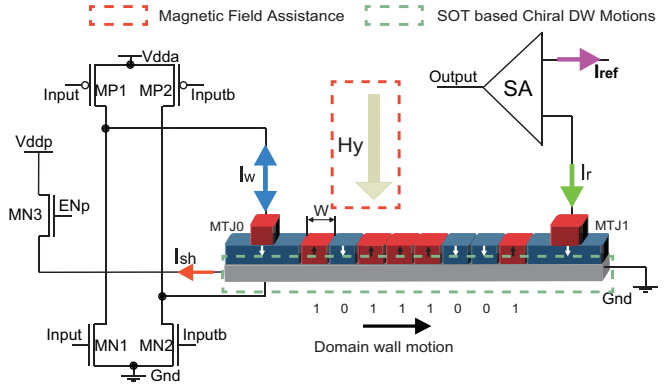

Fig. 1. Racetrack memory based on CIDWM, which is composed of one write head (MTJ0), one read head (MTJ1) and one magnetic nanowire. Writing circuit generates Iw to nucleate data or magnetic domain, propagation circuit generates Ish to induce DW motion and sense amplifier (SA) generates Ir to detect the magnetization direction. (the direction of Ish for the case of SOT should be opposite to that for STT shown in this figure)

Thanks to its multi-bit ability and scalability potential, considerable efforts from academics and industries have been put into the investigation of racetrack memory. The first prototype has been successively fabricated despite of its limited capacity of 256 bits [4]. Meanwhile, this prototype was based on NiFe material with in-plane magnetic anisotropy, which cannot provide a sufficient thermal stability for long data retention in advanced technology nodes below 40 nm. Aiming to tackle this problem, materials with PMA were observed to offer higher energy barrier and show other advantages in terms of current, speed and power consumption.

TABLE I. PARAMETERS AND VARIABLES INTEGRATED IN RACETRACK MEMORY ELECTRICAL MODEL (CO/NI)

Parameter	Description	Default Value
α	Gilbert damping constant	0.045
β	Nonadiabatic coefficient	0.02
P	Spin polarization rate	0.49
Ms	Saturation magnetization	0.66 MA/m
H_w	Walker breakdown field	4.4 mT
γ	Gyromagnetic ratio	0.176 THz/T
λ	DW width	10 nm
K_u	Uniaxial anisotropy	0.41 MJ/m^3
TMR	TMR of write head MTJ	120%
$J_{c\_nucleation}$	DW Nucleation critical current density	57 GA/m^2

With this background, racetrack memory based on magnetic nanowire with PMA (e.g. CoFeB/MgO, Co/Ni, etc.) was proposed [16]. In order to confirm the functionality of this concept and extend it to other optimizations, we develop a SPICE-compatible electrical model. It integrates several critical physics, for example, one-dimension model to describe DW motions shown as follows:

$$\dot{\varphi}_0 + \alpha \dot{X} / \lambda = \gamma H + \beta u / \lambda + f_{pin} \quad (1)$$

$$\dot{X} - \alpha \lambda \dot{\varphi}_0 = v_\perp \sin 2\varphi_0 + u \quad (2)$$

where X is the position of a DW, and φ_0 is the angle that the DW magnetization forms with the easy plane. λ is the width of DW, α is the Gilbert damping constant, β is the dissipative correction to the STT, H is the external field, γ is the gyromagnetic ratio, f_{pin} is the pinning force. The velocity constant $v_\perp$ comes from the hard-axis magnetic anisotropy K_u. u is spin current velocity. Moreover, numbers of experimental parameters (Co/Ni as an example shown in Tab.I) have also been involved. By using this electrical model, ones can design and analyze more complex logic and memory circuits [18].

Beyond the thermal stability issue, the capacity limitation is the most fatal bottleneck hindering the application of racetrack memory. Indeed, high current density required for CIDWMs and high resistivity of magnetic nanowire are two key reasons. In the following, we will present two alternative solutions to improve the capacity.

III. MAGNETIC FIELD ASSISTED AND CHIRAL DOMAIN WALL MOTION BASED RACETRACK MEMORIES

Recent experimental progress showed that magnetic field would trigger DW motions below intrinsic current threshold due to Walker breakdown effect [9]. This observation offers a promising orientation to relieve the pressure of high current density, i.e. magnetic field assisted racetrack memory. Through adding metal lines or coils, an approximately global magnetic field is generated (the magnetic field Hy shown in the red dash square in Fig. 1) [5-6].

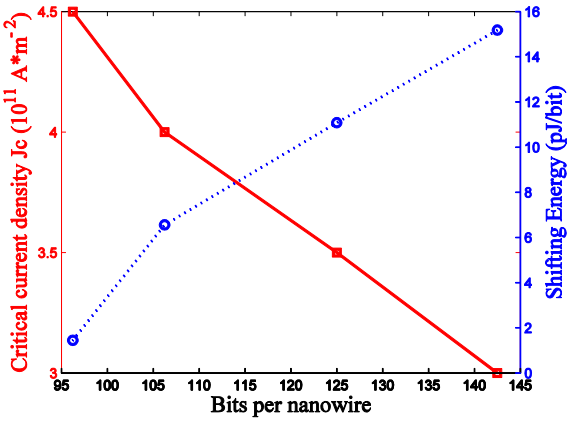

Fig. 2. Dependence of critical current density required and shifting energy versus different number of bits per nanowire in magnetic field assisted racetrack memory.

Due to this field, the current threshold for DW motions in Co/Ni material could be reduced to 3.2 x 10^{11} Am^{-2} rather than the intrinsic one 4.5 x 10^{11} Am^{-2}. By fixing the voltage supply

to 3V and the distance between two adjacent DWs to 40 nm, the limit value of bits per nanowire can exceed 100 and reach up to 150. However, the generation of magnetic field deteriorate overall power consumption. Fig. 2 shows our analyses about the relation among storage capacity, critical shifting current and power consumption. We can find that there is a tradeoff when improving the storage capacity: more bits stored per racetrack memory require lower critical current and more energy consumption.

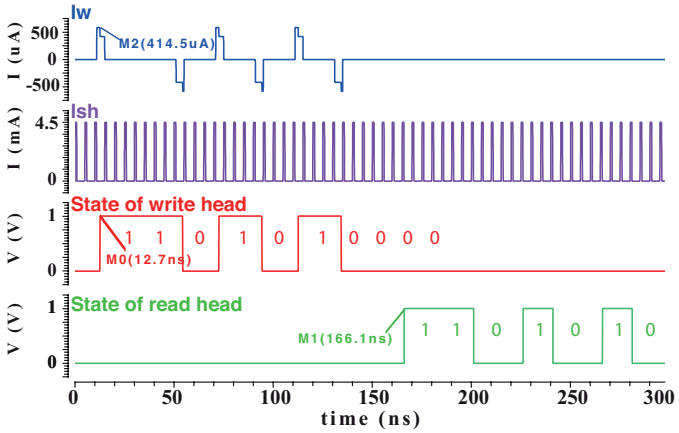

Fig. 3. Transient simulation of 16-bit racetrack memory based on chiral DW motions. Iw is used for inputting data, Ish is used for DW shifting.

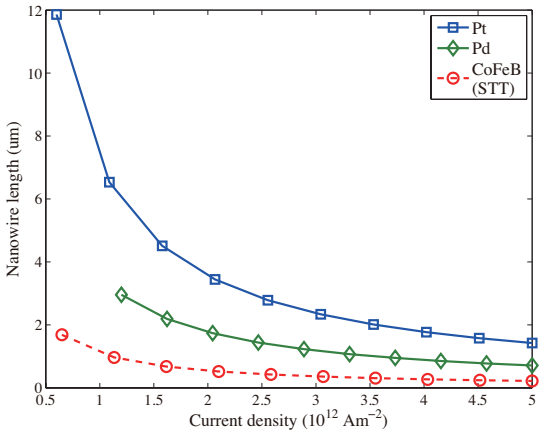

Fig. 4. Dependence of nanowire length versus DW shifting current density for Pt and Pd. Dash line shows the case for the conventional STT based CoFeB racetrack memory.

On the other hand, the SOT based chiral DW motions demonstrates an unprecedented efficient magnetization switching and a high shifting speed. Opposite to STT based CIDWMs, the direction of chiral DW motion is the same with that of applied current. Although it still needs a relatively high current density for DW motions, the nanowire length is increased thanks to the low resistivity of current-flowing non-magnetic materials (e.g. Pt, Pd, etc.) [19-20]. Therefore, chiral DW motions could be another promising solution to improve the capacity of racetrack memory. By adding a non-magnetic layer underneath the magnetic storage nanowire, the concept of racetrack memory based on chiral DW motions is illustrated in Fig. 1 with the green dash square [21]. We validate its functionality with transient simulation of a 16-bit example. As shown in Fig. 3, the data inputted at write head can totally be detected by read head. In order to reveal its prospect for capacity improvement, we compare two non-magnetic materials, Pt and Pd, with conventional STT based CoFeB case. From the result shown in Fig. 4, we find that the proposed racetrack memory design can provide longer nanowire than conventional one with the same current density. Especially, Pt, with the smallest resistivity (1.56×10^{-7} Ω.m), exhibits an obviously high limit among all.

IV. System Level Evaluation

To demonstrate the benefits of using racetrack memory in system level, we replace a SRAM based L2 cache with a racetrack memory based cache. We use gem5 [22], a cycle accurate full system simulator, to simulate PARSEC [23] benchmark suite for performance and power evaluation. All benchmarks are fully executed and we count the overall execution time of the system to evaluate the performance. For energy evaluation, we collect the number of operations of each benchmark and calculate the energy with parameters from a circuit level simulation framework [24]. The system is configured with 4 simple cores, private 32KB I/D cache, and a shared L2 cache. In order to compare an on situ replacement, we conduct an iso-area comparison. We use the 4M SRAM (~ $6.5mm^2$) to compare with 64MB racetrack memory (~$6.2mm^2$). The detailed configurations are shown in Table II.

TABLE II. System Level Experiment Setup Details

Component	Configuration
Processor	4 simple cores, 2GHz, 1-way issue
L1 I/D Cache	32/32KB, 2-way, 64B line, private, LRU SRAM, 1/1 cycle, 6.2/2.3pJ
L2 Cache	16-way, 64B, shared, LRU SRAM: 2MB, 10/10 cycle, 0.57/0.54nJ, 3438mW RM: 64MB, 9/20/5 cycle, 0.50/0.55/0.50nJ, 1062mW
Main Memory	8GB, DDR3, 1600MHz, 120cycle, 12.8GB/s

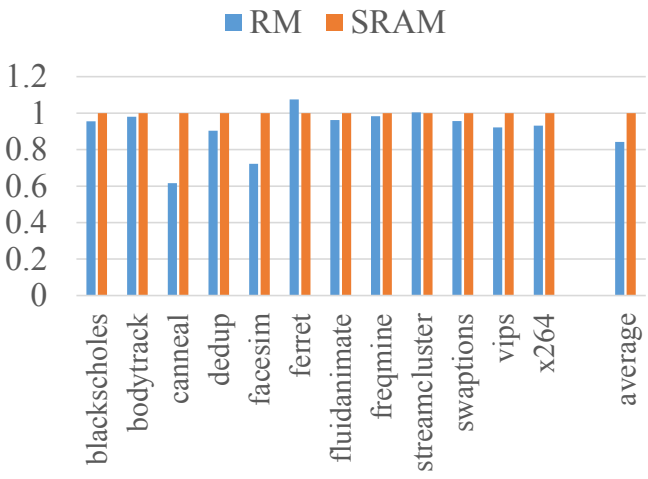

Fig. 5. Comparison of system overall execution time. (RM: racetrack memory)

The overall system performance is shown in Fig. 5. Due to the increase of cache capacity, some benchmarks (e.g. canneal) show significant performance improvement. But some benchmarks (e.g. ferret) suffer from performance degradation due to extra shift latency, which induces about 7.5% overhead. The maximum performance improvement can be up to 38.3%, and the average improvement is 15.8%.

The results of energy consumption are shown in Fig. 6. Generally, racetrack memory reduces the energy consumed in L2 cache. Even though the dynamic energy for racetrack memory is higher than SRAM, the static leakage power of racetrack memory is much lower. Thus racetrack memory reduces the L2 cache energy up to 79.3%, and 73.0% on average. Thus, the replacement will finally reduce the system power consumption.

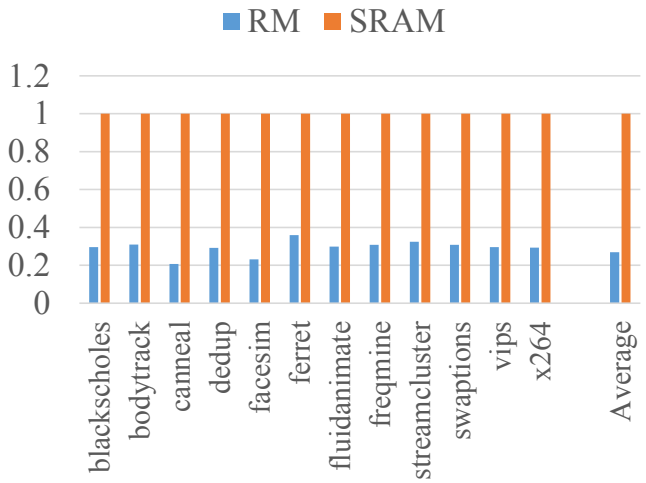

Fig. 6. Comparison of L2 cache energy. (RM: racetrack memory)

V. CONCLUSION

This paper presents the prospect of racetrack memory through the viewpoints from device design to system evaluation. Firstly, two alternative ways to improve the capacity have been proposed. Magnetic field assistance that takes advantage of Walker breakdown effect could reduce required current density. Chiral DW motions provide a new mechanism to achieve racetrack memory and the related materials have lower resistivity compared with conventional STT based CIDWMs. The improvement of capacity could make racetrack memory device more attractive for those systems requiring large on-chop memory. By implementing system-level evaluations, racetrack memory demonstrates its assets in terms of system execution performance and energy consumption.

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