北京大学“信息技术与信息化”名家讲坛

Addressing the General Purpose Processor Dilemma with Reconfigurable Logic Computing

演讲嘉宾：美国麻省理工学院（MIT）Joel Emer教授

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报告摘要：

There recently has been progress in addressing the dilemma between providing programmability and higher performance via an interesting middle ground between fully general-purpose computing and dedicated logic. In specific, reconfigurable logic, typically in the form of FPGAs, addresses many of the cost-related liabilities of dedicated logic and is increasingly being applied to general computation problems.

In this talk, we will examine the possibilities for reconfigurable logic as an ingredient of general-purpose computation. We will look at its potential and attempt to provide an analogy between the state of reconfigurable logic computing today and the early days of conventional computing. In that light, we consider how reconfigurable logic might recapitulate the history of general-purpose computation by looking at how it can fit into the architectural framework that we have generally reserved for conventional processors, how it can be more seamlessly be incorporated into a system and how reconfigurable logic might be made more efficient and be more effectively programmed by looking at the semantic gap between programming languages and the compute fabric itself.

嘉宾简介：

Joel Emer is an Intel Fellow and Director of Microarchitecture Research at Intel in Hudson, Massachusetts and is a Professor of the Practice at MIT. He received his PhD in electrical engineering at the University of Illinois at Urbana-Champaign in 1979. He is a Fellow of both the ACM and the IEEE. He has also received a number of awards including the 2009 Eckert-Mauchly award for lifetime contributions in computer architecture.

Previously he worked at Compaq and Digital Equipment Corporation where he held various researches and advanced development positions investigating processor micro-architecture for a variety of VAX and Alpha processors and developing performance modeling and evaluation techniques. His research included pioneering efforts in simultaneous multithreading, processor reliability analysis and early contributions on the now pervasive quantitative approach to processor evaluation. His current research interests include memory hierarchy design, reconfigurable logic-based computation and performance modeling.